

Serial No.: 09/916,039

REMARKS

Claims 1-2, 4-10, 12-16, 20-28, 30-34, and 36-37 were pending in the application. In response to the office action, applicants have amended claims 1, 4, 9, 12, 15, 24, 28, 30, 34, and 36, and added new claims 38-45. Claims 1-2, 4-10, 12-16, 20-28, 30-34, and 36-45 are now pending for reconsideration.

No fees are believed due with the new claims. However, the commissioner is authorized to charge any additional fees or underpayments to deposit account number 50-0221.

Claims 1-2, 4-10, 12-16, 20-28, 30-34 and 36-37 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,889,819 (Arnett). Claims 4, 12, 30, and 36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Arnett in view of U.S. Patent No. 6,144,242 (Jeong). Applicants have amended the claims to obviate this rejection.

In particular, applicants have amended claims 1, 9, 15, 24, 28, and 34 to recite that the bus or interconnect includes at least two distinct selected binary digital signals to be encoded. Arnett does not teach or suggest this claim recitation.

In contrast to the present claims, Arnett describes EMI reduction for a single synchronous digital signal, such as a clock signal and does not teach or suggest any applicability to high width busses or interconnects, such as digital video interfaces.

With respect to claims 6, 14, 21, and 27, each of these claims recite more than one pseudo-random pattern generator to generate more than one pseudo-random pattern. Applicants have amended the claims to clarify that the more than one patterns are generated and applied to encode the signals prior to transmission. For example, for a high bandwidth transmission, it may be useful to have a different pseudo-random pattern applied to different sub-groupings of the bits (e.g. a first pattern for the first group of 8 bits of a 24 bit video signal, a second pattern for the second group of 8 bits of the signal,

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and a third pattern for the third group of 8 bits of the signal). Arnett is silent in this regard. The two envelope signal generators shown in Fig. 6 involve an encoder on the transmission side and a decoder on the receiving side.

With respect to claims 4, 12, 30, and 36, applicants first note that these claims appear to be inadvertently included in the § 102 rejection. If the rejections are maintained, the Examiner should correct the statement of the rejection.

Applicants have added new claims 38-45 which are believed to be patentable over Arnett and Jeong. Specifically, in some embodiments of the present invention, the random signal may be transmitted along with the encoded signals, simplifying decoding on the receiving end. In Arnett, the envelope signal 20 is routed separately from the encoded signal 14 (see col. 7, lines 2-7). Likewise, the circuits in Arnett appear to lack the synchronizing aspect as recited in the new claims.

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

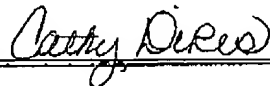
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October 3, 2005
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I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office at (571) 273-8300 on October 3, 2005.

Cathy Dikes



Date: October 3, 2005

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